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MIXED SIGNAL RECEIVER-ON-A-CHIP
RF Front-End Receiver-on-a-Chip

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14. ABSTRACT

The primary goal for the RoC project is to demonstrate highly integrated mixed signal ICs employing the advanced silicon germanium (SiGe) technology. To that end, the MSDT designed two integrated chipsets for a double down conversion receiver architecture with frequency operation ranging from X to L Bands. This report describes the first integrated chipset (IC1) of the receiver block. The updated system architecture of IC1 and the associated layout, shown in Figures 4 and 5, illustrates a single down conversion configuration operating from X to S-Band. Components in IC1 are X-Band Low noise amplifier, lead lag balun, balanced amplifier, double-balanced diode mixer, bandpass filter, and a buffer amplifier. The IC1 chip was packaged in a Precision Multi-Chip Module technology (P-MCM) using the flip chip fabrication process. Measurements of the packaged IC1 chip, shown in Figure 6, achieved 22-23 dB gain across the first IF frequency of 3.7-4.3 GHz.

The targeted application for the SiGe chipset is the Scalable Panels for Efficient and Affordable Radar and UAV programs where the primary drivers are reduction in cost, size, and power while maintaining performance. The successful demonstration of the SiGe chip represents a first pass design success of a highly complex receiver front-end chipset with State of the Art performance.

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RF Front-End Receiver-On-A-Chip Demonstration

In-House Work Unit - 2002IH04

Objective:
The objective of this effort is for AFRL/SND to work in conjunction with MIT Lincoln Laboratory on a cooperative, comprehensive program targeted at technologies, circuits and applications that enable and demonstrate efficient, mixed-signal microsystems. This program is to develop radar module technologies to create a receiver on a chip (RoC) with an emphasis on addressing the needs of future X and S band radar system.

Approach:
The target sub-system is a digital receiver which can be broken into three blocks of functionality and types of signal representations or domain. They are RF front-end, down-converter and analog-to-digital conversion (analog), and data signal processing (digital). The yearly milestones are provided:

1. FY03/04- Design, Test, Characterize and Model High Frequency Test Structures and Passive Components (Model Development/Validation).
2. FY04/05- Model Implementation, Design, Test, Characterize highly integrated RoC Components (LNA, Filter, Mixer, VCO etc.) and Incorporate NeoCAD Tools
3. FY05/06- Design, Test, Characterize Integrated Components and Packaged ROC interfaced, Validate NeoCAD models, tools, and tool flow

Progress:
1. Demonstrated first pass success for X-Band front end receiver. Measurements show ~ 20dB gain for the packaged IC1 SiGe chipset which consists of 6 RF components.
2. Demonstrated first pass success using MIT Lincoln Laboratory's Precision Multi Chip Module (P-MCM) flip chip bonding process that will permit full integration of the entire RF front-end for receiver applications.
3. Demonstrated first pass success for IC2 with measurements of the packaged chip, showing 28.63 dB gain at 1 GHz.

Status:
During the week of 21 Dec. 2004, the AFRL/SND Mixed Signal Team in collaboration with Boeing, Lincoln Labs, and Cadence Design Systems received from fabrication a set of highly complex receiver RF front-end ICs suitable for future DoD phase-array radar applications. The initial results are very promising where the simulated performance matches very closely the actual measured data. The team designed two RFIC chips totaling 16 components based on IBM's 7HP silicon germanium (SiGe) technology where the cutoff frequency (F_t) and the maximum frequency of oscillation (F_{max}) are 120 GHz and 100 GHz, respectively. These designs were submitted to the DARPA sponsored multi-project fabrication run through the trusted foundry process. The system architecture, shown in Fig. 1, illustrates a double down conversion topology ranging from

X to L-Band operation. Components currently undergoing test are LNA, filters, buffer amplifiers, mixers, and splitters. In addition, 26 test structures are also included in the mask to provide additional information concerning the SiGe BICMOS technology. These test structures will be characterized and analyzed for guidance toward future design iterations. The layout of AFRL's ICs and test structures, shown in Fig. 2, requires 80 mm^2 of area resulting in one-quarter of the full reticle size. The targeted application for the SiGe chipset is the MDA/AS RST program's Scalable Panel for Affordable and Efficient Radar and the AF UAV programs where the primary drivers are reduction in cost, size, and power. For prototype demonstration, these chips will next be packaged in a precision multi-chip-module (P-MCM) process at Lincoln Laboratory. Figure 3 is an illustration of the packaging concept showing the entire receiver module of 1 in^2 with a total DC power dissipation of less than 1-Watt. The successful demonstration of the mixed-signal ICs represent the most complex design reported for the advanced SiGe technology for microwave applications.

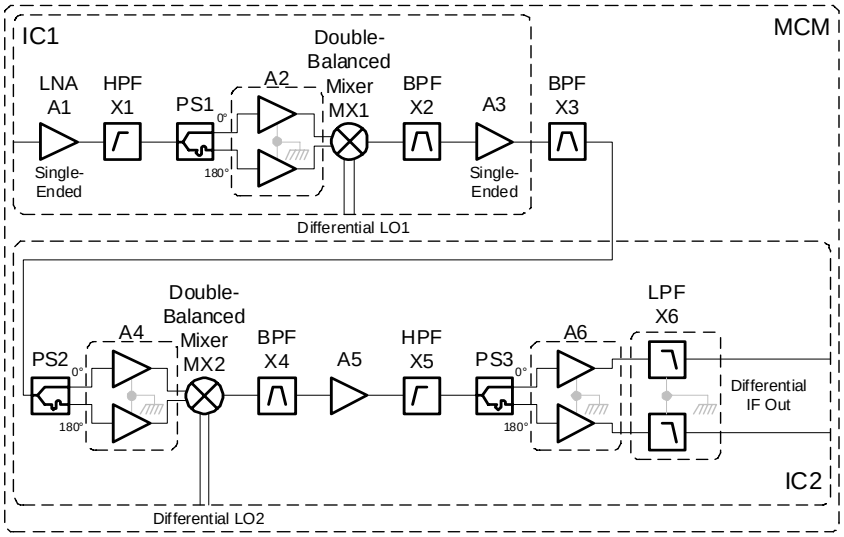

Fig. 1. Notional block diagram of the receiver RF front-end.

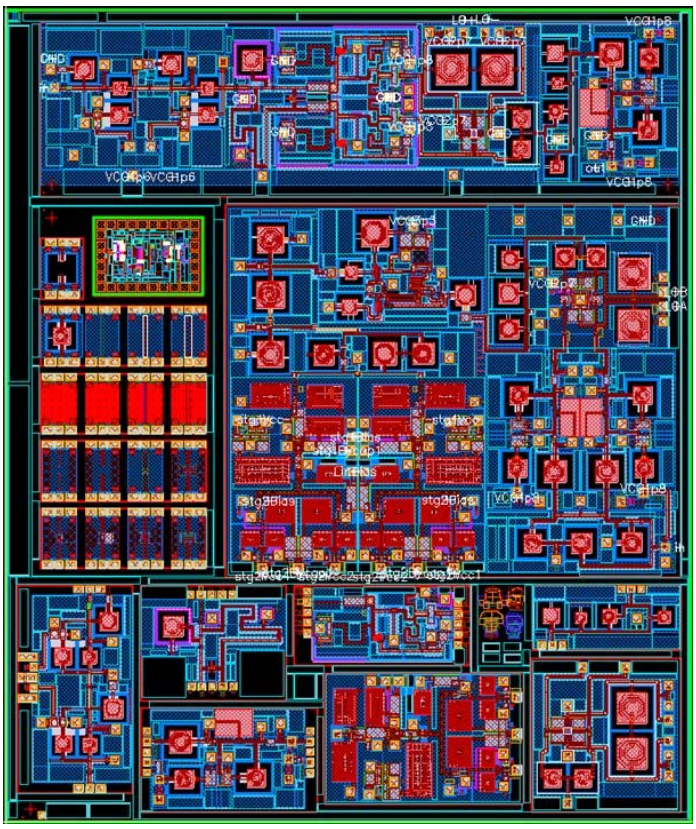

Fig. 2. Layout of the receiver front-end chipset showing the X to S-Band chipset (IC1), S to L-Band chipset (IC2), Dropout 1, and dropout 2.

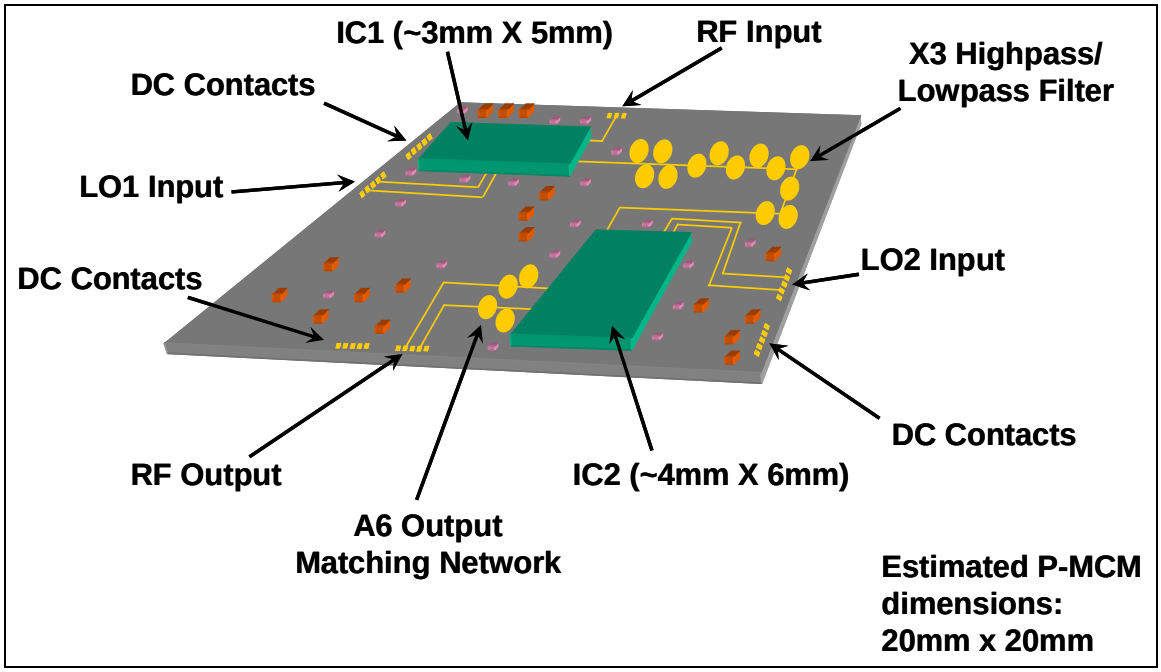

Fig. 3. Illustration of the packaged RFICs in P-MCM technology.

In May 2005, the AFRL Mixed Signal Design Team (MSDT) in collaboration with Boeing Aerospace, MIT Lincoln Laboratory, and Cadence Systems has successfully demonstrated a highly complex receiver RF front-end integrated chipset suitable for future DoD phase-array radar applications. For this effort, individual team responsibilities are: (1) Boeing is responsible for system architecture development and circuit design, (2) MIT Lincoln Laboratory is responsible for packaging and measurement verification, (3) Cadence is responsible for mixed signal tool development / support, and (4) AFRL MSDT is responsible for the program management, circuit design, integration, layout, tool evaluation, and measurement.

The primary goal for the RoC project is to demonstrate highly integrated mixed signal ICs employing the advanced silicon germanium (SiGe) technology. To that end, the MSDT designed two integrated chipsets for a double down conversion receiver architecture with frequency operation ranging from X to L Bands. This report describes the first integrated chipset (IC1) of the receiver block. The updated system architecture of IC1 and the associated layout, shown in Figures 4 & 5, illustrates a single down conversion configuration operating from X to S-Band. Components in IC1 are X-Band Low noise amplifier, lead lag balun, balanced amplifier, double-balanced diode mixer, bandpass filter, and a buffer amplifier. The IC1 chip was packaged in a Precision Multi-Chip Module technology (P-MCM) using the flip chip fabrication process. Measurements of the packaged IC1 chip, shown in Figure 6, achieved 22-23 dB gain across the first IF frequency of 3.7-4.3 GHz.

The targeted application for the SiGe chipset is the Scalable Panels for Efficient and Affordable Radar and UAV programs where the primary drivers are reduction in cost, size, and power while maintaining performance. The successful demonstration of the SiGe chip represents a first pass design success of a highly complex receiver front-end chipset with State of the Art performance.

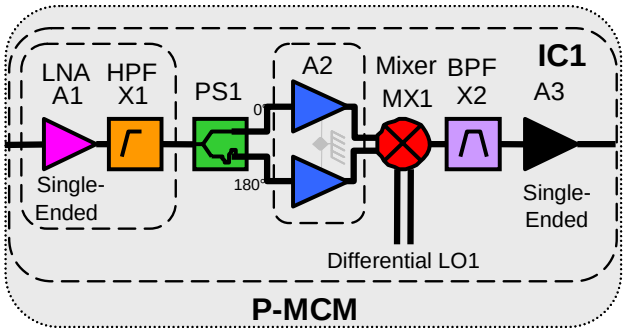

Fig. 4. Block diagram showing IC1 components.

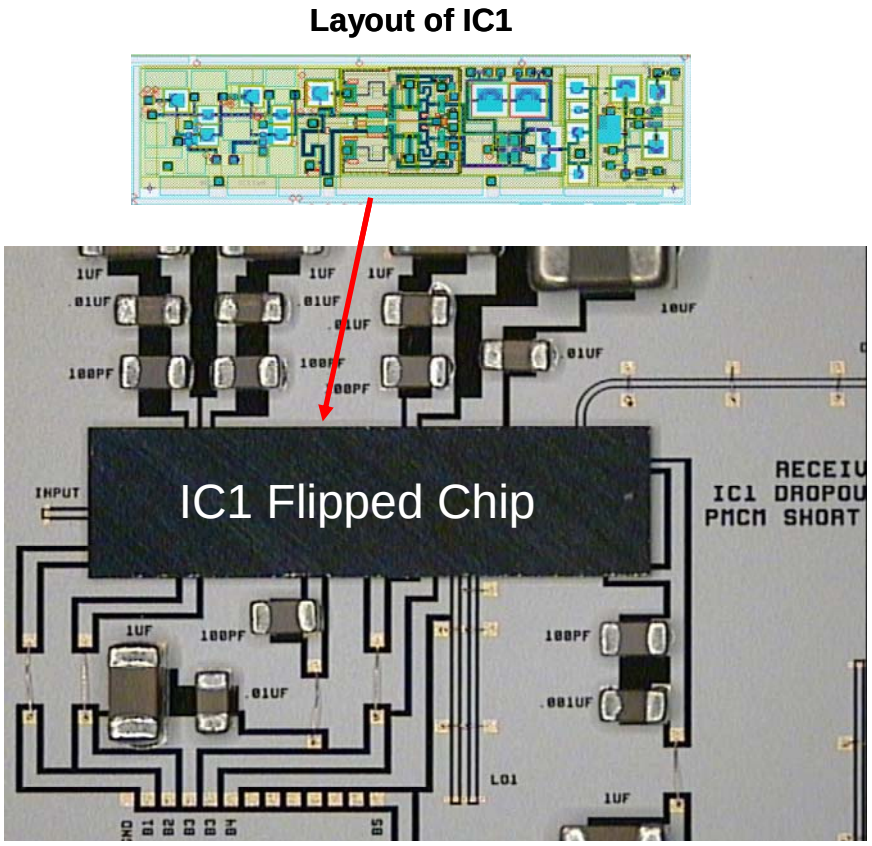

Fig. 5. Photograph of the packaged IC1 in the P-MCM substrate. The top portion of the photograph illustrates IC1 layout.

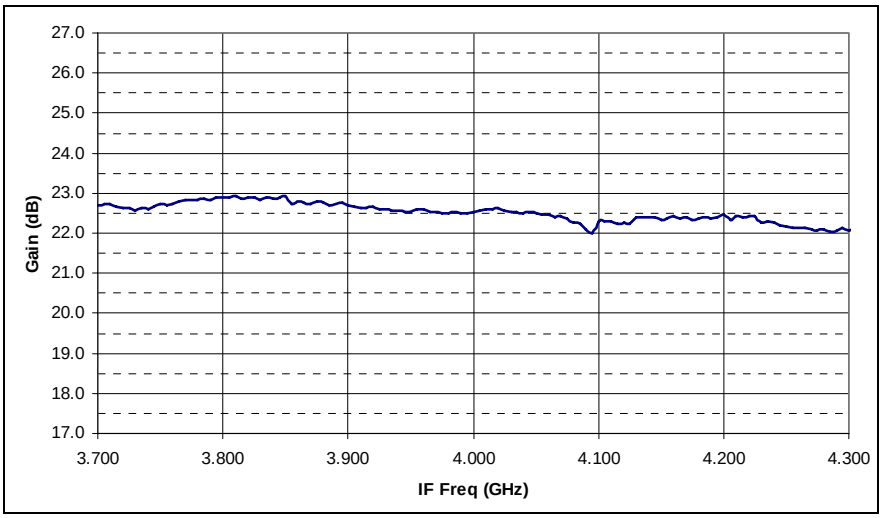

Fig. 6. IC1 Gain measured data showing 1 dB gain flatness across the IF frequency of 3.7-4.3 GHz.

In May 2006, AFRL/SND successfully demonstrated a highly complex receiver RF front-end integrated chipset suitable for future DoD phase-array radar applications. The primary goal of the RoC project is to demonstrate highly integrated mixed signal ICs employing the advanced silicon germanium (SiGe) technology. To that end, the AFRL team designed two integrated chipsets for a double down conversion receiver architecture with frequency operation ranging from X to L Band. The first chip, called IC1, operates from X to S Band was demonstrated earlier achieving 23 dB gain at 4 GHz. This report describes the second integrated chipset (IC2) of the receiver block. The system architecture of IC2 and the associated layout, shown in Figures 7 & 8, illustrate a single down conversion configuration operating from S to L-Band. Components in IC2 are: lead lag splitters (PS2 & PS3), balanced amplifier (A4), double-balanced diode mixer (MX2), non-reflective bandpass filter (X4), buffer amplifier (A5), and an ultra-linear amplifier (A6). Figure 9, illustrates an IC2 chip packaged on a Precision Multi-Chip Module (P-MCM) using the flip chip fabrication process at MIT Lincoln Laboratory. Measurements of the packaged IC2 chip, shown in Figure 10, achieved 28.63 dB gain at 1 GHz. The plot in figure 4 depicts IC2 gain measurement using an Agilent spectrum analyzer where Pin (4GHz) = -30 dBm and LO (3GHz) = 6 dBm.

The targeted application for the receiver / exciter SiGe chipset is the Digital Beam Forming Scalable Panel for Affordable and Efficient Radar and UAV programs where the primary drivers are reduction in cost, size, and power. The successful demonstration of the SiGe chip represents a first pass design success of a highly complex receiver front-end chip with SOA performance.

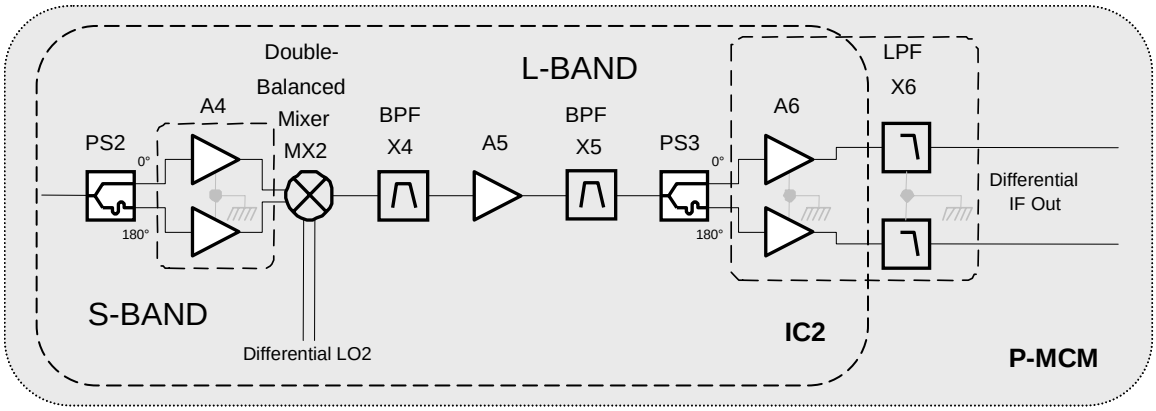

Figure7. Block diagram showing IC2 components.

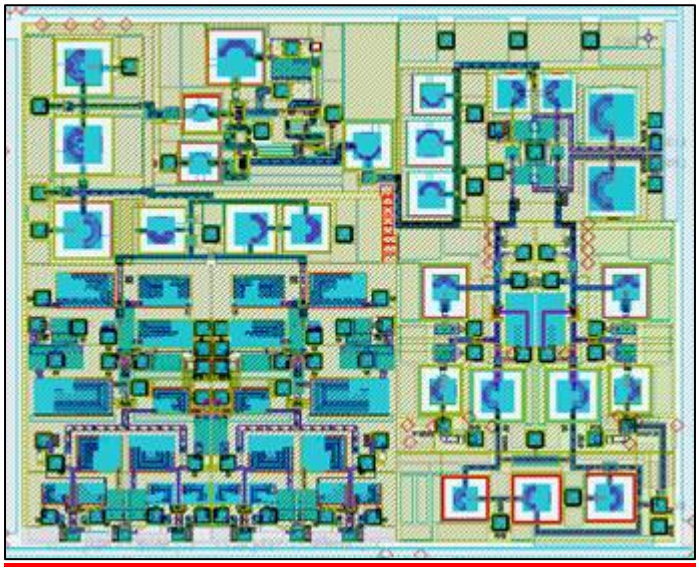

Figure 8. Layout of the SiGe IC2 chipset.

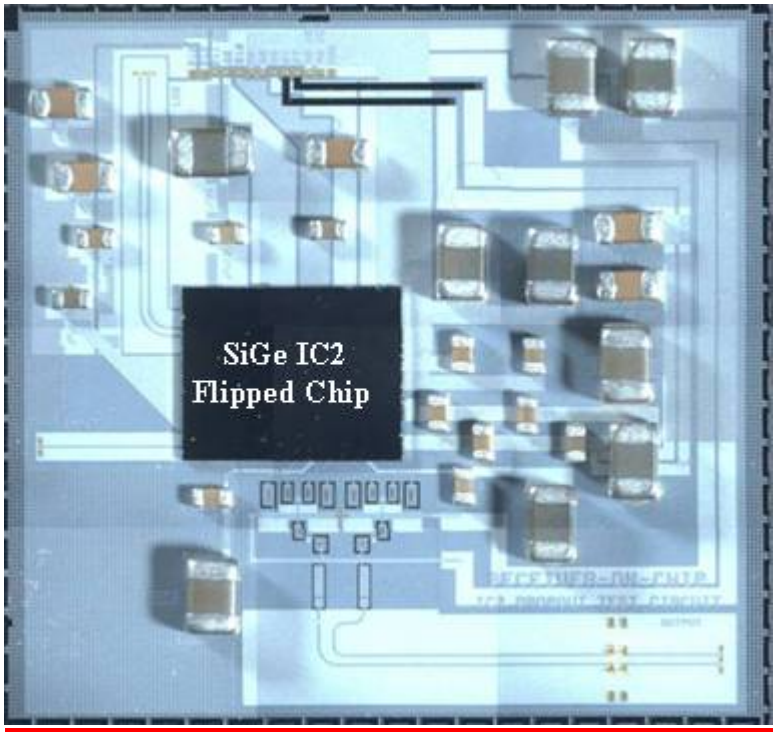

Figure 9. Photograph of the packaged IC2 chip on the P-MCM substrate.

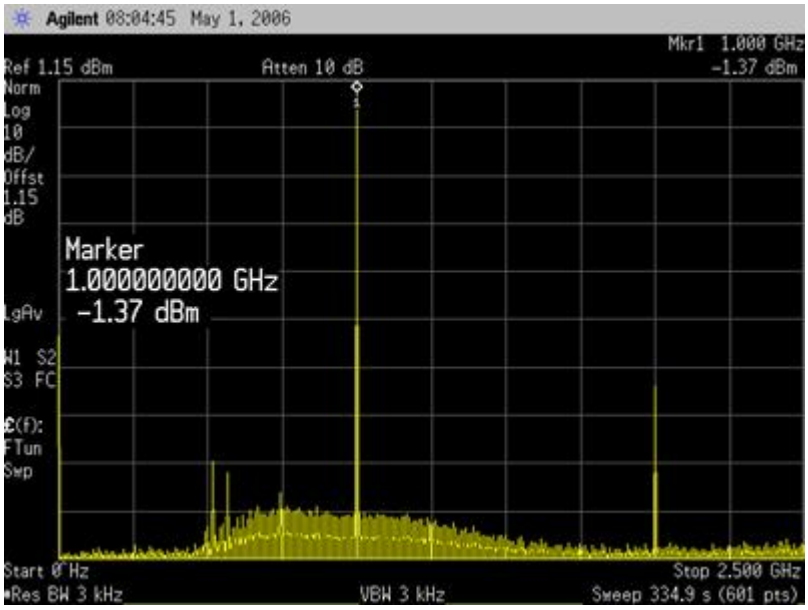

Figure 10. IC2 Gain measured data showing 1 GHz data.
For this measurement, Pin = -30 dBm & Pout = -1.37 dBm, resulting in 28.63 dB gain.

Future Plans:
In the Summer of 2006, both IC1 and IC2 are to be packaged with a MAX108 analog to digital converter and the complete integrated X-Band receiver fully characterized.